

Multicore Computer Architecture - Storage and Interconnects

Tutorial 2

Cache Memory



NPTEL Online Course : Multi-Core Computer Architecture and Interconnects Dr. John Jose, IIT Guwahati

Dr. John Jose

Assistant Professor

**Department of Computer Science & Engineering
Indian Institute of Technology Guwahati, Assam.**

Tutorial Problem-1

- ❖ For a 32KB direct mapped cache with 128 byte cache block, give the address of the starting byte of the first word in the block that contains the following address. (a) 0X A23847EF

Tutorial Problem-2

- ❖ A cache has 256 KB capacity, 1B word, 128 byte block size and 4 way set associative. The system is using 32 bit address. Given the following addresses, which set of cache will be searched and specify which byte of the selected cache block will be forwarded if it is a hit in cache? (a) 0XABC89987

Tutorial Problem-3

- ❖ It takes 2.5 ns to access a tag array value and 4 ns to access a data array, 1 ns to perform hit/ miss comparison and 1ns to return the selected data to processor. (a) What is the cache hit latency of the system? (b) What would be the hit latency of the system if both tag and data array access take 2.5 ns and hit/ miss comparison take 1 ns?

Tutorial Problem-4

- ❖ A cache has hit rate = 95%, 128 byte block, cache hit latency = 5ns. Main memory takes 100 ns to return first word (32 bits) of a block and 10 ns for each subsequent word. What is the miss latency of the cache? What is average memory access time ?

Tutorial Problem-5

- ❖ Assume a 2-level cache system with the following specifications.
L1 Hit Time = 1 cycle, L1 Miss Rate = 2.5%, L2 Hit Time = 6 cycles, L2 Miss Rate = 10% (% L1 misses that miss), L2 Miss Penalty = 120 cycles.
Compute the average memory access time.

**THANK
YOU!**



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johnjose@iitg.ac.in
<http://www.iitg.ac.in/johnjose/>